IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Ariel Cohen et al.		
Assignee:	LSI Logic Corporation		
Title:	USE OF INTERNAL GENERAL PURPOSE REGISTERS OF A PROCESSOR AS A JAVA VIRTUAL MACHINE TOP OF STACK AND DYNAMIC ALLOCATION OF THESE REGISTERS ACCORDING TO STACK STATUS		
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Commissioner for Patents
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DECLARATION OF STEVEN M. EMERSON PURSUANT TO 37 C.F.R. § 1.132

I, Steven M. Emerson hereby declare as follows:

1. I am presently employed as an Engineering Manager of the Processor Cores Technology Group by LSI Logic Corporation ("LSI Logic").

2 I have been employed by LSI Logic since Jun 95 in various capacities.

3. A copy of my curriculum vitae is attached to this declaration.

4. I have reviewed the relevant portions of the specification and the claims of the present invention, the relevant portions of the relevant Office Action, and the relevant portions of U.S. Patent No. 6,332,215 to Patel et al. and U.S. Patent No. 6,021,469 to Tremblay et al.

5. I understand that in one embodiment the present invention concerns:

An apparatus comprising:

a processor (i) comprising a number of internal general purpose registers and (ii) configured to manipulate contents of said internal general purpose registers in response to instruction codes of a first instruction set;

a processor interface circuit coupled to said processor;

a memory interface circuit coupled to a memory device;

an extension stack coupled between said processor interface and said memory interface and configured to (i) receive data from and present data to said memory interface circuit and (ii) receive data from and present data to said processor interface circuit; and

a translator circuit (i) coupled between said processor interface and said memory interface and (ii) configured to implement a stack using one or more of said internal general purpose registers of said processor and said extension stack.

6. I understand that in another embodiment the present invention concerns:

An apparatus comprising:

means for manipulating data in response to instruction codes of a first instruction set, said manipulating means comprising a number of internal general purpose registers; and

means for translating instruction codes of a second instruction set into sequences of said instruction codes of said first instruction set, wherein said translating means is configured to (i) implement a stack with one or more of said internal general purpose registers and an extension stack coupled between said manipulating means and a memory device, (ii) use said one or more of said internal general purpose registers as a top of stack, (iii) empty said extension stack to said memory device, (iv) refill said extension stack from said memory device, (v) transfer contents of said one or more internal general purpose registers to said extension stack and (vi) transfer contents of said extension stack to said one or more internal general purpose registers.

7. I understand that in another embodiment the present invention concerns:

A method for implementing a Java virtual machine top of stack comprising the steps of:

(A) translating one or more instruction codes of a first instruction set into sequences of instruction codes of a second instruction set;

(B) manipulating contents of one or more internal general purpose registers of a processor in response to said sequence of instruction codes of said second instruction set; and

(C) implementing a stack comprising said one or more internal general purpose registers and an extension stack coupled between said processor and a memory device, wherein said one or more internal general purpose registers are configured as a top of stack and said extension stack is configured to (i) receive data from and present data to said memory device and (ii) receive data from and present data to said processor.

8. U.S. Patent No. 6,332,215 to Patel does not disclose and would not suggest an extension stack as presently claimed.

9. In particular, the JAVA stack 50 of Patel appears to be connected only to the hardware JAVA registers 44 of Patel (see FIG. 3 of Patel). Since Patel shows the JAVA stack 50 only connected to the hardware registers 44, it follows that Patel does not disclose or suggest an extension stack coupled between the processor interface and the memory interface and configured to (i) receive data from and present data to said memory interface circuit and (ii) receive data from and present data to said processor interface circuit, as presently claimed.

10. Patel states that the Java registers are part of the Java Virtual Machine and should not be confused with general registers 46 or 48 which are operated upon by the central processing unit 26 (see column 4, lines 35-38 of Patel).

11. Element 44 in FIG. 3 of Patel is described as hardware Java registers that store the Java registers defined by the Java Virtual Machine (see column 4, lines 6-12 of Patel).

12. Since Element 44 in FIG. 3 of Patel represents hardware Java registers and Patel teaches that Java registers should not be confused with general registers which are operated upon by the central processing unit 26, a person skilled in the field of the present invention would (i) not consider Element 44 in FIG. 3 of Patel to be internal general purpose registers of the

processor 25 of Patel and (ii) not consider the processor 25 of Patel as being configured to manipulate contents of the hardware Java registers 44 of Patel.

13. FIG. 3 of Patel shows data (i.e., output of the instruction cache 24) moving only from the instruction cache 24 to (i) the Java accelerator 42 or (ii) the processor 25.

14. FIG. 3 of Patel shows data (i.e., output of the Java accelerator 42) moving only from the Java accelerator 42 to the processor 25 (i.e., via multiplexer 28).

15. Patel teaches that data (i.e., byte code instructions) is received from the instruction cache 24 in response to the Java PC or the normal program counter 54.

16. A person of ordinary skill in the field of the present invention would consider the Java PC and normal program counter to be addresses used to retrieve data from the instruction cache 24.

17. A person of ordinary skill in the field of the invention would consider using addresses to retrieve data from a memory to be different from presenting data to the memory as presently claimed.

18. Since Patel only shows information moving (i) from the instruction cache 24 and (ii) to the processor 25, a person skilled in the field of the presently claimed invention would not

consider either Element 44 or Element 50 to be configured to (i) receive data from a processor and (ii) present data to a memory, as presently claimed.

19. The statement in Patel that "The Java registers in the Java Virtual machine include ... Frame, a pointer to the execution environment of the current method (column 4, lines 12-17 of Patel) does not disclose and would not suggest to one or ordinary skill in the field of the present invention an extension stack comprises both head and tail interfaces, as presently claimed.

20. Based on the description in column 4, lines 19-22 of Patel of the Java stack 50 and the CPU associated register files 46 and 48, a person of ordinary skill in the field of the invention would understand the hardware Java stack 50 as being an alternative to storing the stack in the CPU associated register files.

21. The positions taken in the Office Action (see page 2, section 5 and page 6, section 17 of the Office Action mailed January 12, 2005) that the element 44 in FIG. 3 of Patel corresponds to both (i) the presently claimed internal general purpose registers and (ii) the presently claimed register block coupled between the processor interface circuit and the extension stack are not supported by the disclosure of Patel.

22. I hereby declare that all statements made herein of my knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or patents issued therefrom.

Date: 5/12/05

Steven M. Emerson